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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,960	01/02/2002	Jeffrey R. Wilcox	ITL-0668US	2148

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Timothy N. Trop
TROP, PRUNER & HU, P.C.
8554 KATY FWY, STE 100
HOUSTON, TX 77024-1805

EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,960	WILCOX ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-14,21-26,29,30,34-36 and 40-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-14, 21-26, 29-30, 34-36, and 40-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 1 September 2004. Claims 1-7, 15-20, 27-28, 31-33, and 37-39 are canceled. Claims 8-14, 21-26, 29-30, 34-36, and 40-42 are pending. Applicants' arguments have been carefully and respectfully considered in light of the instant amendment, and some are persuasive, while others are not, as will be discussed in more detail below. Accordingly, this action has been made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8-14, 21-26, 29-30, 34-36, and 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Taruishi et al (U.S. Patent 6,339,552).

The claims "read on" a method and apparatus disclosed by Taruishi et al, and thus the invention as broadly set forth in the claims is seen to be anticipated by Taruishi et al.

More specifically, with respect to claims 8, 21, 29, 34-36, and 40-42, Taruishi et al (U.S. 6,339,552) disclose a method and apparatus for controlling amplification in a

memory of a computer system so as to reduce power consumption, as in the claimed invention.

Taruishi et al discloses providing amplifiers for amplifying data signals from a memory bus. (Taruishi et al disclose that sense amplifiers within data I/0 circuits (DIO0-DIO3) in Figure 1 are used to amplify data signals from a memory bus, as discussed in column 5, lines 59-64, e.g.

Providing a "first circuit" for "sampling" the amplified data signals (a data output circuit 4 in Figure 1 may be used to "sample" the amplified data signals, e.g.).

Taruishi et al further teach providing ("second") circuitry for selectively enabling and disabling the amplification in response [to] an edge (claims do not specify rising or falling, although in the DDR disclosed by Taurishi et al in column 10, lines 5-10, it may be both edges) of said at least one data strobe signal in column 9, lines 7-9, column 10, lines 5-10 and column 11, lines 25-27. Column 6, lines 35-40 discuss the fact that the invention of Taurishi et al, the, "...sense amplifiers... are not activated for the non-selected memory banks." Accordingly, the sense amplifiers are activated for the selected bank and word line, as is discussed in columns 9 and 10. Therefore, the amplifiers are, in fact, enabled in response to an edge of a data strobe signal (DQS).

Attention is also respectfully directed to column 2, lines 24-41 and 57-62, column 4, lines 39-51; and column 12, lines 1-16.

(Note that reference is made to U.S. Patent 6,339,552 (which is an English language patent family member of JP 2001-067877) for convenience.)

Also with respect to claims 29, 34, and 40, Taruishi et al disclose that the memory may be utilized in a computer system such as a microcomputer which, as one of ordinary skill in the art would recognize, includes some sort of processor which initiates a predetermined operation with the memory using a clock signal and the various "commands" or instructions discussed throughout Taruishi et al (see column 17, lines 45-47, as well as column 8, lines 16+, e.g.).

With respect to claim 9, Taruishi et al teach that the "selectively disabling" comprises selectively disabling sense amplifiers (again see column 6, lines 33-40, e.g.).

With respect to claims 10 and 22, Taruishi et al teach that the "selectively disabling" and "selectively enabling" comprises selectively enabling sense amplifiers as discussed above (again see column 6, lines 33-40). The selective enabling and disabling of the sense amplifiers in Taruishi et al may be considered to occur in response to the beginning and end of a "predetermined" operation such as when a particular bank is selected/deselected for a read or write operation, i.e. the enabling of the sense amplifiers is performed in response to the beginning of a read/write operation when a bank is selected for operation and the disabling of the sense amplifiers is performed in response to the end or completion of a particular predetermined operation such as a read or write operation when a bank is deselected.

With respect to claim 12, Taruishi et al also teach "communicating" signals associated with a double data rate (DDR) synchronous dynamic random access memory (SDRAM) device over the memory bus (see column 1, lines 5-10 and column 5, lines 13-15, e.g.) Also, see column 10, lines 5-10.

With respect to claims 13-14, 23-24, and 30, the operation for which a particular bank may be selected in Taruishi et al may be a read or write operation, as discussed in column 7, lines 30-60, where the DQS is supplied as a write strobe signal upon a write operation, and is outputted as a read strobe signal.

With respect to claim 11, Taruishi et al teach that data input and output and input operations may be synchronized to the edge of a data strobe signal that appears on a memory bus in connection with the predetermined operation (again see column 7, lines 32-59, e.g.).

With respect to claim 25, the apparatus of Taruishi et al includes circuitry for controlling various components of a memory and thus the "apparatus" of Taruishi et al may be broadly considered to be a memory "controller."

With respect to claim 26, Taruishi et al teach that the apparatus may comprise a memory device such as an SDRAM device as discussed above (again see column 1, lines 5-10 and column 5, lines 13-15, e.g.).

Response to Arguments

With respect to applicants' argument that Taruishi et al fail to teach all limitations of independent claims 8, 21, 29, 34, and 40, and thus, fail to anticipate these claims, examiner respectfully disagrees.

More specifically, with respect to independent claims 8 and 34, the claims now recite enabling the amplification of data signals in response to an edge of at least one strobe signal. Applicants argue that contrary to these claim limitations, Taruishi et al disclose enabling a control signal (called DIE) in response to a write command that is

communicated to a memory device. Examiner notes that while this may or may not be true, it is irrelevant, as it is not what anticipates applicants' claimed invention, as discussed supra. Taruishi et al disclose a data strobe signal (DQS) that enables amplification in response to an edge of said at least one data strobe signal, as is discussed in more detail supra with respect to claims 8, 21, 29, 34, and 40, for example.

More specifically with respect to independent claims 21, 29, and 40, applicants argue that Taruishi et al disclose activating an input data latch in response to the detection of a write command, not in response to an edge of a data strobe signal. As applicants do not cite any portion of Taruishi et al to support their argument, define their definition of a "write command" to eliminate the DQS as discussed above from being considered one, and examiner cannot find citations in Taruishi et al himself to support that argument, examiner must respectfully disagree, and, again, refer applicants to the rejection of the claims supra.

Therefore, Taruishi et al teach the amended limitations of independent claims 8, 21, 29, 34, and 40, as discussed supra with respect to same.

With respect to applicants' arguments that neither Huang nor the AAPA teach or suggest the claim limitations of 8, 21, 29, 34, or 40, examiner respectfully agrees, and has removed the rejections accordingly.

Specifically, examiner agrees that Huang does not explicitly recite enabling an amplifier in response to an edge of a data strobe signal, a deficiency not made up for by AAPA.

Therefore, the 35 USC 103 rejections applied previously have been removed by examiner in light of the arguments presented in light of the instant amendments to the claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703.308.1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian P. Chace